What is claimed is:

1. An input buffer receiver comprising:

a buffer input portion for receiving an input signal SIGNAL_IN;

a large capacitance between a PMOS bias node and a VSS source voltage; and

a buffer output portion for producing an output signal SIGNAL_OUT1.

2. The input buffer receiver of claim 1, wherein the buffer input portion which receives an input signal SIGNAL_IN comprises:

a first transistor N11 having a source node to which a VSS source voltage is applied, a gate node to which a reference voltage VREF is applied, and a drain node to which a signal VB11 is applied;

a second transistor P11 having a drain node which is connected to the drain node of the first transistor N11, and a gate node to which a signal VB11 is applied, and a source node to which an upper supply voltage VDD is applied;

a third transistor P12 having a drain node which is connected to the drain of

a fourth transistor N12, a gate node to which a signal VB11 is applied, and a source node to which an upper supply voltage VDD is applied;

a fourth transistor N12 having a source node to which a VSS source voltage is applied, a gate node to which an input signal SIGNAL_IN is applied externally, and a drain node which is the input to the buffer output portion.

3. The input buffer receiver of claim 1, wherein the first and fourth transistors, N11 and N12, are NMOS transistors, and the second and third transistors, P11 and P12, are PMOS transistors.

4. The input buffer receiver of claim 1, wherein the large capacitance is connected between the sources of the first and fourth transistors, N11 and N12, of the buffer input portion and the gate of the second transistor P11 of the buffer input portion.

5. The input buffer receiver of claim 1, wherein the gate of the second transistor P11 is connected to its drain.

6. The input buffer receiver of claim 1, wherein the gate of the second transistor P11 is connected to the drain of the first transistor N11.

7. The input buffer receiver of claim 1, wherein the gate of the second transistor P11 is connected to the gate of the third transistor P12.

8. The input buffer receiver of claim 1, wherein the buffer output portion which produces an output signal SIGNAL_OUT1 comprises:
a first inverter I11 connected to the drain of the third transistor P12 and the drain of the fourth transistor N12;

9. The input buffer receiver of claim 1, wherein P12 and N12 activate almost simultaneously to provide an efficient circuit design technique for filtering ground noise.

10. The input buffer receiver of claim 1, involving a large capacitance coupling ratio, which charge couples the PMOS bias node of the input buffer receiver to the VSS source voltage of the input buffer receiver.

11. The input buffer receiver of claim 1, involving a large capacitance coupling ratio, which results in a quicker response time for a SIGNAL_OUT1.